dream SAM3703

LOW POWER LOW COST EFFECT PROCESSOR

Real-time audio applications…

- Effect processing (reverb, echo, chorus, …)
- MP3 decoding
- Filtering, sampling rate conversion

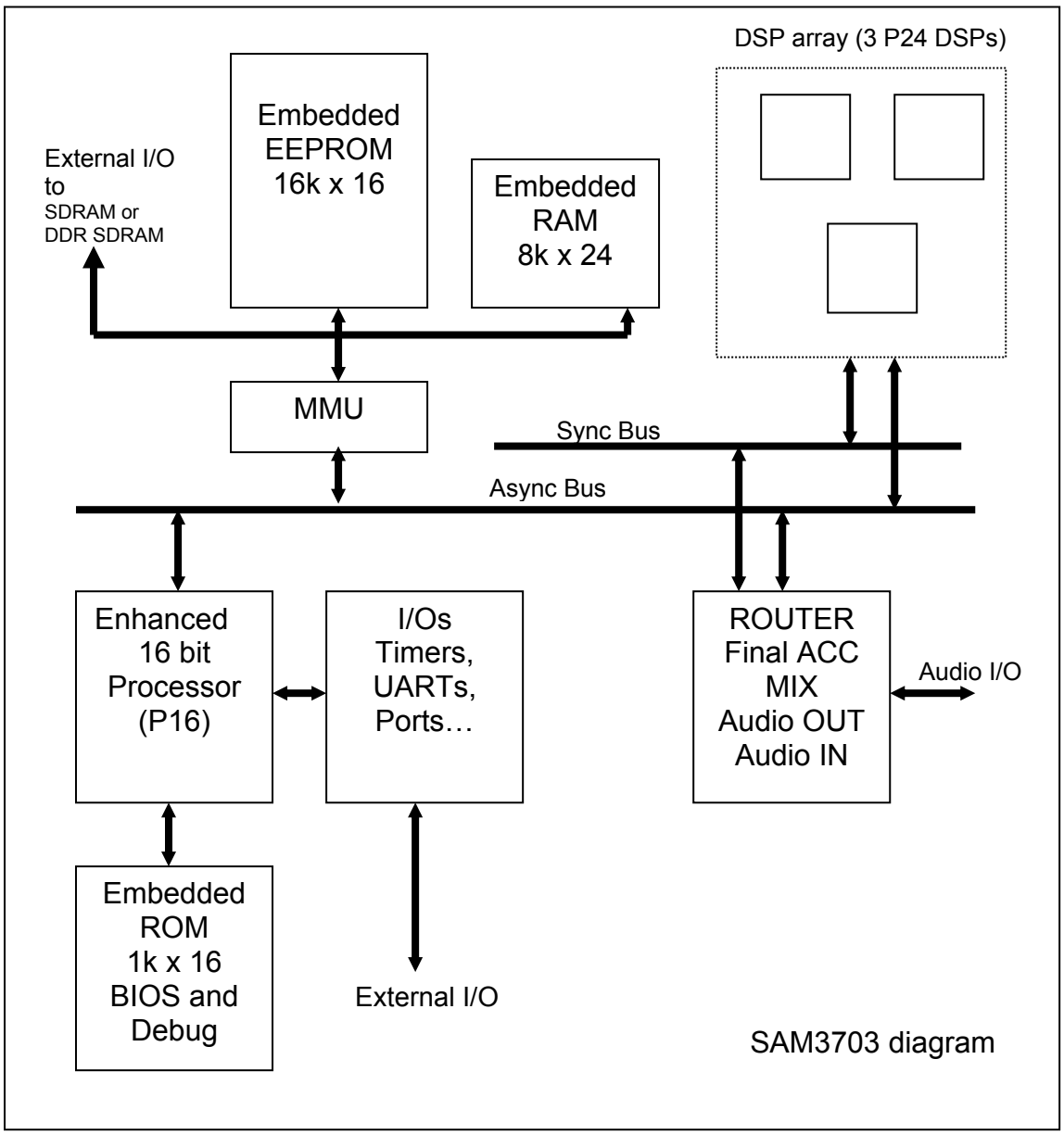
for audio products…

- Professional audio
- Consumer electronic
- MP3 Player

at the best performance / price.

- 3 DSPs and 24-bit Audio Router on chip
- 32kHz to 96kHz sampling rate
- Enhanced P16 processor with C compiler
- New 48 bit double precision DSP instructions
- Built-in 16k x 16 flash memory
- Built-in 8k x 24 RAM
- Secure Code – Copy protected
- Direct connection of LEDs, switches
- Direct connection of LCD display
- 8 channels audio in + out
- DDR-SDRAM / SDRAM support in burst mode
- MIDI In/Out
- 8-bit parallel interface
- Warm start power-down
- Deep Power Down (<5µA) using built-in power switch
- LQFP80 package

1. Dream DSP Array Overview



The SAM3703 is a new member of the SAM3000 family of sound synthesis/processing ICs that uses the DSP array technology. It is designed for superior quality sound processing. The 16-bit processor has new instructions and a C compiler for quicker reliable firmware development. Total compatibility is maintained with the other members of the family. Applications written for the SAM3703 can be burned into the built-in Flash memory. This memory has specific features to avoid external read of the coded data, thus ensuring very effective copy protection.
The minimum configuration for a product is SAM3703 + Codec. An external SDRAM/DDR-SDRAM is needed if 8k internal RAM is not sufficient for extended delay line buffers, like high-quality reverb.

- DSP Array

The SAM3703 includes 3 on-chip DSPs.
Each DSP (P24) is built around a 2k x 24 RAM and a 1k x 24 ROM. The RAM contains both data and P24 instructions; the ROM contains typical coefficients such as FFT cosines and windowing. A P24 sends and receives audio samples through the Sync Bus. It can request external data such as compressed audio through the Async Bus. Each P24 RAM can be accessed through the Async Bus.
Each P24 is capable of typical MAC operation loops, including auto-indexing, bit reverse and butterfly (multiplication of complex numbers). It also includes specialized audio instructions such as state variable IIR filtering, envelope generation, linear interpolation and wavetable loop. The DSP's have new 48-bit double precision instructions for improved Pro Audio applications.
One P24 is sufficient for processing one channel of MP3, implementing a multi-tap delay line or a multi-tap transversal filter.

- Sync Bus

The Sync Bus transfers data on a frame basis, typical frame rates being 32, 44.1, 48, 96 kHz. Each frame is divided into 64 time slots. Each slot is divided into 4 bus cycles. Each P24 is assigned a hardwired time slot (8 to 63), during which it may provide 24-bit data to the bus (up to 4 data samples). Each P24 can read data on the bus at any time, allowing inter P24 communication at the current sampling rate. Slots 0 to 7 are reserved for a specific router DSP, which also handles audio out, audio in, and remix send.

- Async Bus

The Async Bus is 24-bit data inside the chip and 16-bit outside.
The P16 processor normally masters the Async Bus, it can read/write the P24 memories and the external or embedded ROM/RAM. However, each P24 can request a bus master cycle for accessing external ROM/RAM or other P24 memories. This allows efficient intercommunication between several P24s on asynchronous block basis. Specific P24 instructions FLOAT and FIX allow to convert fixed point DSP data to floating point 16 bits. This allows for 20-bit audio dynamic range when using 16-bit external memory.

- Enhanced 16-bit processor

This is the new enhanced version of P16 processor with added instructions allowing optimized use of C compiler. Using the P16, widely used in Dream products, maintains continuity for the large firmware investments from the SAM97xx series. A built-in ROM, connected to the P16 holds basic input/output software (BIOS) for peripherals such as UART, SmartMedia®, MPU, as well as a debugger which uses a dedicated asynchronous serial line. The firmware can reside on the built-in 16k x 16 EEPROM or it can be downloaded at power-up into the built-in 8k x 24 RAM from serial SmartMedia or host.

- MMU (memory management unit)

The MMU handles transfer requests between the external or embedded RAM/ROM, the P16 and the P24s through the Async Bus. The SAM3703 includes an on chip 8k x 24 RAM.

- Router: final ACC, MIX, audio out, audio in

This block includes a RAM, accessed through the Async Bus, which defines the routing from the Sync Bus to/from the Audio I/O or back to the Sync Bus (mix send). It takes care of mix and accumulation from Sync Bus samples. 8 channels of audio in and 8 channels of audio out are provided (4 stereo in/out, I2S format). The stereo audio in channels may have a different sampling rate than the audio out channels. In this case, one or more P24s take care of sampling rate conversion.

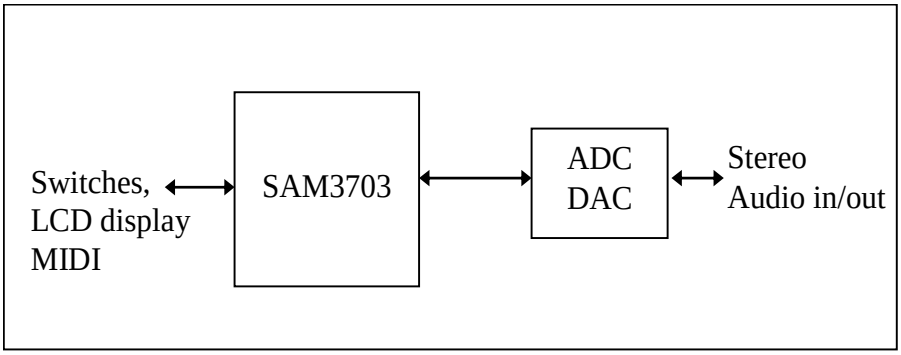
- I/O

The SAM3703 includes very versatile I/Os, that share common pins for reduced pin count and small IC footprint. Most I/Os, when not used for a specific function, remain available as firmware controlled general-purpose pins.
The following peripherals are included on chip:

- 2 x 8-bit timers
- 2 x 16-bit timers
- Parallel slave 8-bit port, MPU401 compatible
- Parallel master 8-bit port, for connection to SmartMedia and/or LCD display, switches, etc.
- 2 x asynchronous bi-directional serial port (one used as debug interface).
- Synchronous serial slave port (SPI type host connection).
- Firmware controlled I/O pins.

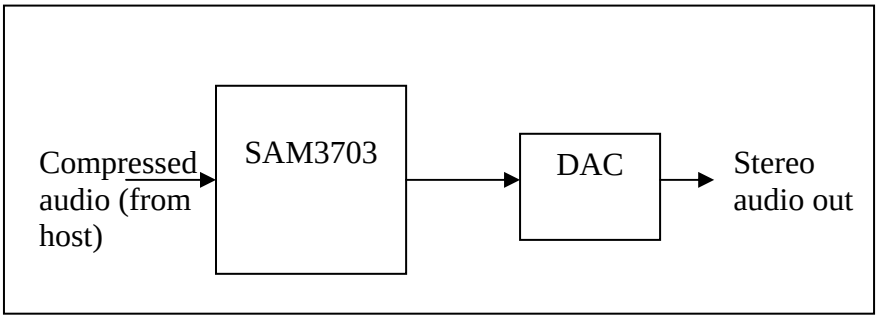
2. Typical application examples

2.1. Low cost, high quality effect



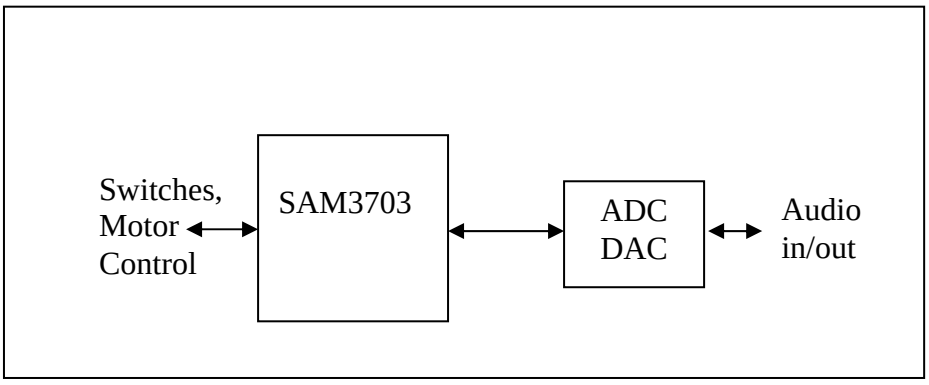
- High quality, full 24-bit Multi-effects like reverb, chorus, compressor…
- Stereo10-band graphic equalizer

2.1. Host controlled MP3 player



- SAM3703 firmware download from host (when using parallel interface).
- Choice of host communication interfaces:
  - 8-bit parallel
  - Asynchronous serial
  - Synchronous serial (SPI)
- Full MP3 support including very low bit rates extension (ISO/IEC 13818-3).
- Easily upgradable to other coding standards.

2.3. Toys with “artificial intelligence”



- Speech recognition
- Learning functions
- ADPCM record / play

3. DSP capacity and I/O configuration

3.1. DSP considerations

The SAM3703 include 3 x P24 DSPs.
The table below lists the performance achievable by the P24:

Function	P24s required
MP3 decode	3
Stereo reverb and chorus @48kHz	1
31-band equalizer @96kHz	3
Stereo 31-band equalizer @48kHz	3

The SAM3703 runs firmware directly from an embedded EEPROM memory. It may also run firmware from local RAM. The SAM3703 is the ideal choice when external components count should be minimized and many I/O pins are required.

3.2. I/O selection considerations

I/Os are organized in groups, which can be mutually exclusive because they share the same IC pins (please refer to the pinout to identify the exclusions). The two main types of operation are host controlled and stand-alone.

3.2.1. Host-controlled operation

There are 3 main ways of communication with a host processor:

- 8-bit parallel MPU type bi-directional interface
  signals: D7-D0, CS/, WR/, RD/, A0, IRQ
- Asynchronous serial, MIDI_IN
- Synchronous serial
  signals: SDIN, SCLK, SYNC, INT/

3.2.2. Stand-alone operation

Possible stand-alone modes are:
- Firmware into built in EEPROM memory
- Firmware into external SmartMedia. In this case, the firmware should reside in the SmartMedia reserved sectors starting at sector # 1.

4. SAM3703

4.1. Pin description

Identical sharing number indicates multifunction pins.
Pd indicates pin with built-in pull-down resistor.
Pu indicates pin with built-in pull-up resistor.
SSTL indicate a SSTL_2 class 1 compliant I/O pin.

Pin name	Pin#	Type	Sharing	Description
GND	1,13,24,32, 40,45,49,54, 61,70	PWR	-	Digital ground. All these pins should be returned to a ground plane
VC18	28,46,62,77	PWR	-	Core power. All these pins should be returned to nominal 1.8V or to PWROUT if the built-in power switch is used.
VC33	4,76	PWR	-	Periphery power. All these pins should be returned to nominal 3.3V.
VC25	22,33,42,50, 55	PWR		Memory PAD Power +2.25V to +3.6V. All VC25 pins should be returned to +2.5V (for DDR SDRAM) or 3.3V (for SDRAM)
PWRIN	59	PWR	-	Power switch input, should be returned to nominal 1.8V even if the power switch is not used
PWROUT	58	PWR	-	Power switch output, should be connected to all VC18 pins if the power switch is used
VREF	41	In		VC25/2 reference for SSTL_2 pins.
D7-D0	10,9,8,7,6,5, 3,2	I/O Pd	1	Slave 8-bit interface data. Output if CS/ and RD/ are low (read from chip), input if CS/ and WR/ are low (write to chip). Type of data defined by A0 input.
I/O7-I/O0	10,9,8,7,6,5, 3,2	I/O Pd	1	SmartMedia data or other peripheral data
P0.7-P0.0	10,9,8,7,6,5, 3,2	I/O Pd	1	General purpose I/O can individually be programmed as input or output
CLAD3-0	10,9,8,7	In Pd	1	Optional bit clocks and word selects for digital audio input. Used for sampling rate conversion, for external incoming digital audio such as AES/EBU or S/PDIF.
WSAD3-0	6,5,3,2	In Pd	1	
A0	16	In	2	Slave 8-bit interface address. Indicates data/status or data/ctrl transfer type (CS/ RD/ low or CS/ WR/ low)
SMPD	16	In	2	SmartMedia presence detect
P0.10	16	In	2	General purpose input pin
SCLK	16	In	2	Serial slave synchronous interface input clock
CS/	12	In Pu	3	Slave 8-bit interface chip select, active low.
P0.11	12	In Pu	3	General purpose input pin
SYNC	12	In Pu	3	Serial slave synchronous interface input sync signal
WR/	17	In Pu	4	Slave 8-bit interface write, active low. D7-D0 data is sampled by chip on WR/ rising edge if CS/ is low
SMC/	17	In Pu	4	SmartMedia configuration. This pin is sensed after power-up. If found low, it is assumed that a SmartMedia connector is present. The built-in firmware will wait for SmartMedia SMPD.
P0.12	17	In Pu	4	General purpose input pin

RD/	18	In Pu	5	Slave 8-bit interface read, active low. D7-D0 data is output when RD/ goes low and CS/ is low
R|B/	18	In Pu	5	SmartMedia Ready Busy/ status
P0.13	18	In Pu	5	General purpose input pin
MIDI_IN	18	In Pu	5	Serial MIDI in
SDIN	18	In Pu	5	Serial slave synchronous interface input data
IRQ	11	Out	6	Slave 8-bit interface interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0)
SMRE/	11	Out	6	SmartMedia read enable (RE/), active low
FS0	11	In	6	Freq sense, sensed at power up. Together with FS1, allows the firmware to know the operating freq of the chip (see FS1)
P0.8	11	I/O	6	General purpose I/O pin
INT/	11	Out	6	Serial slave synchronous interface data request, active low.
DABD0	73	Out		Stereo channel 0 of digital audio output, I2S format
DABD1	74	Out	7	Stereo channel 1 of digital audio output, I2S format
P0.14	74	Out	7	General purpose output pin
DABD2	75	Out	8	Stereo channel 2 of digital audio output, I2S format
P0.15	75	Out	8	General purpose output pin
DABD3	78	Out	9	Stereo channel 3 of digital audio output, I2S format
MIDI_OUT	78	Out	9	Serial MIDI out
DAAD0	66	In Pd	-	Stereo audio data input, I2S format. Can operate on CLBD master rate or CLAD0 or CLAD01 external rate when sampling rate conversion is requested. DAAD0 has built-in pull-down. It may be left open if not used.
DAAD1	67	In Pd	-	Additional channel of stereo audio input, I2S format. Can operate on CLBD master rate or CLAD1 or CLAD01 external rate when sampling rate conversion is requested. DAAD1 has built-in pull-down. It may be left open if not used.
DAAD2	68	In Pd	10	Additional channel of stereo audio input, I2S format. Can operate on CLBD master rate or CLAD2 external rate when sampling rate conversion is requested. DAAD2 has built-in pull-down. It may be left open if not used.
CLAD01	68	In Pd	10	Optional bit clock for digital audio inputs DAAD1-0. Used for sampling rate conversion, for external incoming digital audio such as AES/EBU or S/PDIF.
DAAD3	69	In Pd	11	Additional channel of stereo audio input, I2S format. Can operate on CLBD master rate or CLAD3 external rate when sampling rate conversion is requested. DAAD3 has built-in pull-down. It may be left open if not used.
WSAD01	69	In Pd	11	Optional word select for digital audio inputs DAAD1-0. Used for sampling rate conversion, for external incoming digital audio such as AES/EBU or S/PDIF.
FS1	69	In Pd	11	Freq sense, sensed at power up. FS1|FS0 allow firmware to know operating freq of chip as follows (optional): 00- 6.9552 MHz 01- 9.6 MHz 10- 11.2896 MHz 11- 12.288 MHz
P0.9	69	In Pd	11	General purpose Input pin
CLBD	72	Out	-	Audio bit clock for DABD3-0. Audio bit clock for DAAD3-0 if the corresponding CLAD3-0 is not used.
WSBD	80	Out	-	Audio left/right channel select for DABD3-0. Audio left/right channel for DAAD3-0 if the corresponding WSAD3-0 is not used.

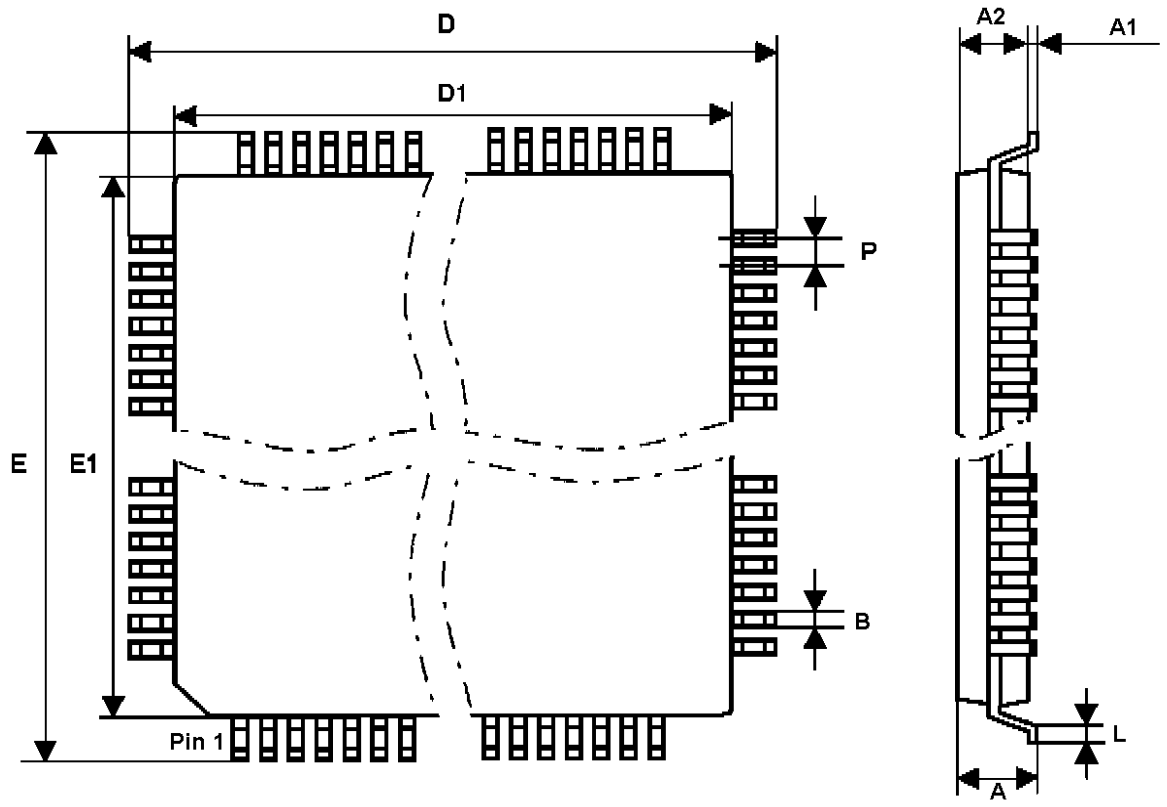
CKOUT	71	Out	-	External DAC/Codec master clock. Same or double frequency as X2 pin. Can be programmed to be 128xFs, 192xFs, 256xFs, 384xFs, 512xFs, Fs being the DAC/Codec sampling rate.
WA11 - WA0	35,34,31,30, 29,27,26,25, 23,21,20,19	Out SSTL	12	Multiplexed addresses for external SDR SDRAM or DDR SDRAM memory
P2.11- P2.0	35,34,31,30, 29,27,26,25, 23,21,20,19	I/O SSTL	12	General purpose I/O pins
WCKE	57	Out SSTL	13	Clock Enable for external SDR SDRAM or DDR SDRAM memory
P2.12	57	I/O SSTL	13	General purpose I/O pin
WBA1 - WBA0	37,36	Out SSTL	14	Bank selects for external SDR SDRAM or DDR SDRAM memory
P2.14 - P2.13	37,36	I/O SSTL	14	General purpose I/O pins
WDQ3	52	I/O SSTL	15	External memory SDR SDRAM or DDR SDRAM data bit 3
P1.3	52	I/O SSTL	15	General purpose I/O pin
SMCE/	52	Out SSTL	15	SmartMedia chip enable (CE/), active low
WDQ2	51	I/O SSTL	16	External memory SDR SDRAM or DDR SDRAM data bit 2
P1.2	51	I/O SSTL	16	General purpose I/O pin
SMALE	51	Out SSTL	16	SmartMedia address latch enable (ALE)
WDQ1	48	I/O SSTL	17	External memory SDR SDRAM or DDR SDRAM data bit 1
P1.1	48	I/O SSTL	17	General purpose I/O pin
SMWE/	48	Out SSTL	17	SmartMedia write enable (WE/), active low
WDQ0	47	I/O SSTL	18	External memory SDR SDRAM or DDR SDRAM data bit 0
P1.0	47	I/O SSTL	18	General purpose I/O pin
SMCLE	47	Out	18	SmartMedia command latch enable (CLE)
WDQS	53	I/O SSTL	19	Data Strobe for external DDR SDRAM memory
P1.4	53	I/O SSTL	19	General purpose I/O pin
WCK	44	Out	20	Positive clock for external SDR SDRAM or DDR SDRAM memory
P1.5	44	I/O	20	General purpose I/O pin
WCK/	43	Out	21	Negative clock for external DDR SDRAM memory
P1.6	43	I/O	21	General purpose I/O pin
WRAS/	39	Out SSTL	22	Row address strobe for external SDR SDRAM or DDR SDRAM memory
P1.7	39	I/O	22	General purpose I/O pin
WCAS/	38	Out SSTL	23	Column address strobe for external SDR SDRAM or DDR SDRAM memory
P1.8	38	I/O	23	General purpose I/O pin
WWE/	56	Out SSTL	24	Write enable for external SDR SDRAM or DDR SDRAM memory
P2.15	56	I/O SSTL	24	General purpose I/O pin

X1 – X2	64,63	-	-	External crystal connection. Standard frequencies are 6.9552 MHz, 9.6 MHz, 11.2896 MHz, 12.288 MHz. Max frequency is 12.5 MHz. An external clock (max. 1.8Vpp) can be connected to X1 using AC coupling (22pF). A built-in PLL multiplies the clock frequency by 4 for internal use.
RESET/	14	In	-	Master reset Schmitt trigger input, active low. RESET/ should be held low during at least 10ms after power is applied. On the rising edge of RESET/, the chip enters an initialization routine, which may involve firmware download from an external SmartMedia, or host.
STIN	65	In Pd	-	Serial test input. This is a 57.6 kbauds asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. STIN has a built-in pull-down. It should be grounded or left open for normal operation.
STOUT	79	Out	-	Serial test output. 57.6 kbauds async output used for firmware debugging.
PDWN/	60	In	-	Power down input, active low. High level on this pin is typ. VC18. When PDWN/ is low, the oscillator and PLL are stopped, the power switch opens, and the chip enters a deep sleep mode (1µA typ. consumption when power switch is used). To exit from power down, PDWN/ has to be set high then RESET/ applied. Alternate programmable power-downs are available which allow warm restart of the chip.
TEST	15	In Pd	-	Test input. Should be grounded or left open.

4.2. Pin-out by pin

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	GND	**21**	WA2 P2.2	**41**	VREF	**61**	GND
2	D0 I/O0 P0.0 WSAD0	**22**	VC25	**42**	VC25	**62**	VC18
3	D1 I/O1 P0.1 WSAD1	**23**	WA3 P2.3	**43**	WCK/ P1.6	**63**	X2
4	VC33	**24**	GND	**44**	WCK P1.5	**64**	X1
5	D2 I/O2 P0.2 WSAD2	**25**	WA4 P2.4	**45**	GND	**65**	STIN
6	D3 I/O3 P0.3 WSAD3	**26**	WA5 P2.5	**46**	VC18	**66**	DAAD0
7	D4 I/O4 P0.4 CLAD0	**27**	WA6 P2.6	**47**	WDQ0 SMCLE P1.0	**67**	DAAD1
8	D5 I/O5 P0.5 CLAD1	**28**	VC18	**48**	WDQ1 SMWE/ P1.1	**68**	DAAD2 CLAD01
9	D6 I/O6 P0.6 CLAD2	**29**	WA7 P2.7	**49**	GND	**69**	DAAD3 WSAD01 FS1 P0.9
10	D7 I/O7 P0.7 CLAD3	**30**	WA8 P2.8	**50**	VC25	**70**	GND
11	IRQ INT/ SMRE/ FS0 P0.8	**31**	WA9 P2.9	**51**	WDQ2 SMALE P1.2	**71**	CKOUT
12	CS/ P0.11 SYNC	**32**	GND	**52**	WDQ3 SMCE/ P1.3	**72**	CLBD
13	GND	**33**	VC25	**53**	WDQS P1.4	**73**	DABD0
14	RESET/	**34**	WA10 P2.10	**54**	GND	**74**	DABD1 P0.14
15	TEST	**35**	WA11 P2.11	**55**	VC25	**75**	DABD2 P0.15
16	A0 SMPD P0.10 SCLK	**36**	WBA0 P2.13	**56**	WWE/ P2.15	**76**	VC33
17	WR/ SMC/ P0.12	**37**	WBA1 P2.14	**57**	WCKE P2.12	**77**	VC18
18	RD/ R|B/ P0.13 MIDI_IN SDIN	**38**	WCAS/ P1.8	**58**	PWROUT	**78**	DABD3 MIDI_OUT
19	WA0 P2.0	**39**	WRAS/ P1.7	**59**	PWRIN	**79**	STOUT
20	WA1 P2.1	**40**	GND	**60**	PDWN/	**80**	WSBD

5. Mechanical dimensions



SAM3703
Thin 80-lead quad flat pack (LQFP80)
Dimensions (mm)

	MIN.	NOM.	MAX.
A	-	1.40	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
L	0.45	0.60	0.75
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
P		0.40	
B	0.13	0.16	0.23

6. Electrical Characteristics

6.1. Absolute Maximum Ratings(*)

Parameter	Symbol	Min	Typ	Max	Unit
Temperature under bias	-	-55	-	+125	°C
Storage temperature	-	-65	-	+150	°C
Voltage on any pin X1,PDWN/	-	-0.3	-	VC18+.3	V
Others	-	-0.3	-	VC33+.3	V
Supply voltage	VC18	-0.3	-	1.95	V
	VC25	-0.3	-	3.6	V
	VC33	-0.3	-	3.6	V
Maximum IOL per I/O pin (excepted SSTL pins)	-	-	-	4	mA
Maximum IOH per I/O pin (excepted SSTL pins)	-	-	-	4	mA
Maximum IOL per SSTL pin - VOUT=VTT-0.405	-	-	-	8	mA
Maximum IOH per SSTL pin - VOUT=VTT+0.405	-	-	-	8	mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VC18	1.65	1.8	1.95	V
Supply voltage (note 1)	VC33	3	3.3	3.6	V
Supply voltage PWRIN pin	PWRIN	1.75	1.9	1.95	V
Operating ambient temperature	tA	0	-	70	°C

Note 1: Operation at lower VC33 values down to VC18 is possible, however external timing may be impaired. Please contact Dream if you plan to use these circuits with VC33 outside the recommended operating range.

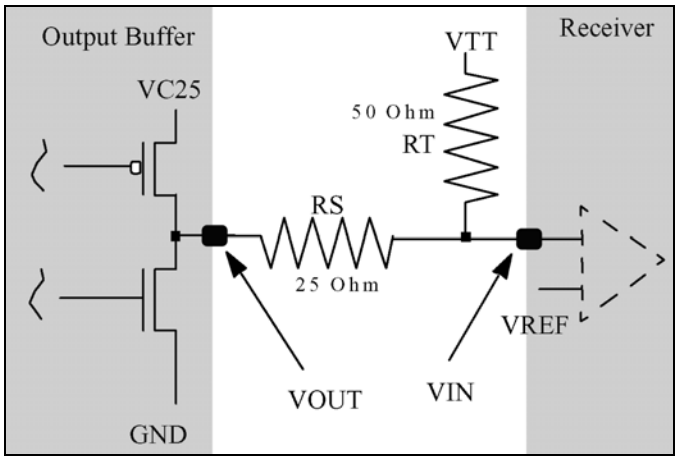
6.2.1. SSTL_2 pads

Memory pads of SAM3703 are SSTL_2 compliant. This feature allows direct interfacing with DDR SDRAM devices.

DDR SDRAM OPERATION

When using DDR SDRAM memory, it is recommended to use the following schematic for Address, Data , and Data Strobe.
In power down mode, the command lines (WRAS/, WCAS/, WWE/, WCKE) have fixed level, contrary to Address and data lines which are floating. To avoid consumption in Power down, RT can be not implemented on command lines.

Typical SSTL_2 Input/Output environment



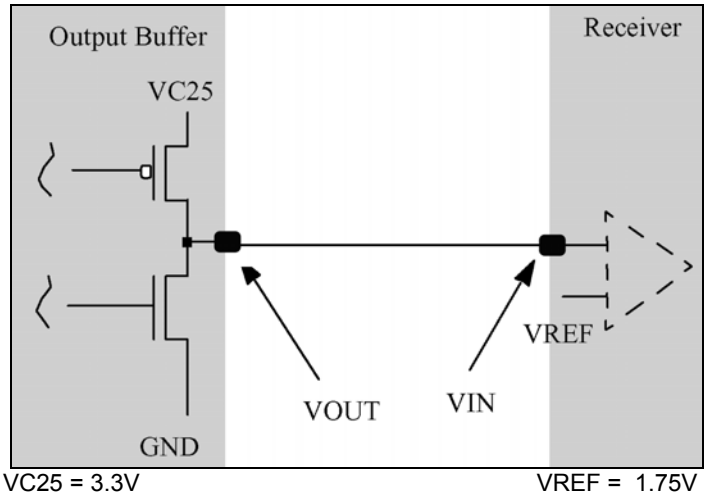
VC25 = 2.5V VREF = 1.25 V
VTT = 1.25V (sink / source capability)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VC25	2.3	2.5	2.75	V
Reference voltage	VREF	VC25/2 - 0.04	1.25	VC25/2 + 0.04	V
Serial resistor	RS	22.5	25	27.5	Ohm
Termination resistor	RT	45	50	55	Ohm

For more detail about SSTL_2, please refer to the EIA/JEDEC standard EIA/JESD8-9

SDR SDRAM OR GPIO OPERATION

When using SSTL_2 pad as SDR SDRAM or GPIO signals, it is recommended to use the following schematic.



VC25 = 3.3V VREF = 1.75V

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VC25	3	3.3	3.6	V
Reference voltage	VREF	VC25/2 - 0.04	1.65	VC25/2 + 0.04	V

6.2.2. D.C. Characteristics

(TA=25°C, VC18=1.8V±10%, VC33=3.3V±10%, VC25=2.5V±10%)

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage, except X1, PDWN/ and SSTL pads	VIL	-0.3	-	0.8	V
High level input voltage, except X1, PDWN/ and SSTL pads	VIH	2	-	3.6	V
Low level input voltage SSTL pads	VIL	-	-	VREF-0.31	V
High level input voltage SSTL pads	VIH	VREF+0.31	-	-	V
Low level input voltage X1, PDWN/	VIL	-0.3	-	0.605	V
High level input voltage X1, PDWN/	VIH	1.235	-	VC18+0.3	V
Low level output voltage IOL=-2mA (Memory pads excepted)	VOL	-	-	0.4	V
High level output voltage IOH=2mA (SSTL pads excepted)	VOH	VC33-0.4	-	-	V
Low level output voltage IOL=-2mA (SSTL pads only)	VOL	-	-	0.4	V
High level output voltage IOH=2mA (SSTL pads only)	VOH	VC25-0.4	-	-	V
VC18 power supply current (crystal freq.=12.288 MHz, all 3 P24 running)	IC18	-	27	-	mA
VC18 power supply current (crystal freq. = 12.288 MHz, all P24 stopped, warm start power-down active)	IC18	-	4	-	mA
VC18 deep power down supply current (using power switch)	IC18	-	1	10	µA
VC33 power supply current (crystal freq.= 12.288 MHz)	IC33	-	1	-	mA
VC25 power supply current (crystal freq.= 12.288 MHz, SDRAM controller Off)	IC25	-	0	-	mA
VC25 power supply current (crystal freq.= 12.288 MHz, SDRAM controller On, RS=25, RT=50)	IC25	-	75	-	mA
Built-in pull-up / pull-down resistor	PU/PD	10	-	56	kOhm

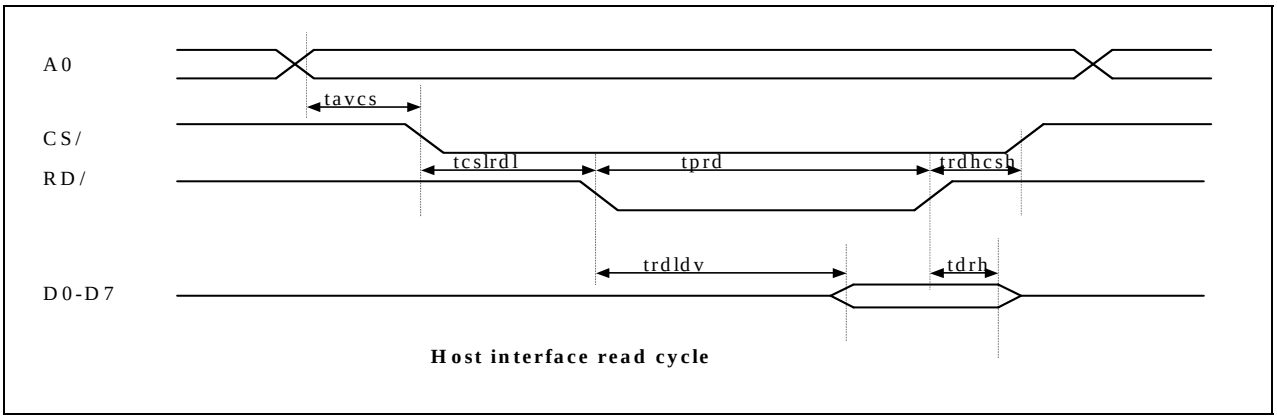
7. Peripherals and Timings

A built-in PLL multiplies the Xtal clock frequency by 4 for internal use. plck is the period of the internal clock generated by PLL. plck = tck/4. Typical value with Xtal 12.288 MHz is plck = 20.34 ns.

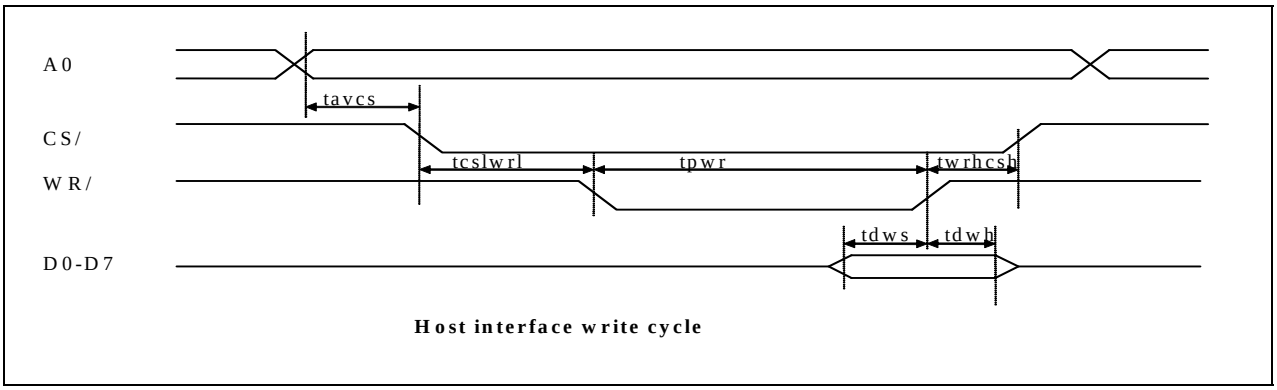
7.1. Slave 8bit parallel interface

Pins used: D7-D0 (I/O), CS/ (input), A0 (input), WR/ (input), RD/ (input), IRQ (output)
This interface is typically used to connect the chip to a host processor.

- Timings



Host interface read cycle



Host interface write cycle

Parameter	Symbol	Min	Typ	Max	Unit
Address valid to chip select low	tavcs	0	-	-	ns
Chip select low to RD/ low	tcslrdl	5	-	-	ns
RD/ high to CS/ high	trdhcsh	5	-	-	ns
RD/ pulse width	tprd	50	-	-	ns
Data out valid from RD/	trdldv	-	-	20	ns
Data out hold from RD/	tdrh	1.7	-	10	ns
Chip select low to WR/ low	tcslwrl	5	-	-	ns
WR/ high to CS/ high	twrhcsh	5	-	-	ns
WR/ pulse width	tpwr	50	-	-	ns
Write data setup time	tdws	10	-	-	ns
Write data hold time	tdwh	0.9	-	-	ns

- IO Status Register

TE	RF	X	X	X	X	X	X

Status register is read when A0 = 1, RD/ = 0, CS/ = 0

TE: Transmit empty. If 0, data from SAM3703 to host is pending and IRQ is high. Reading the data at A0=0 sets TE to 1 and clear IRQ.
RF: Receiver full. If 0 then SAM3703 is ready to accept DATA from host.

Note: If status bit RF is not checked by host, write cycle time should not be lower than 3µs.

7.2. SmartMedia and other peripheral interface

This is a master 8-bit parallel interface, allowing connection to SmartMedia or other peripherals such as LCD screens.

Pins used:
I/O7-I/O0 (I/O)
SMPD (input)
SMCE/, SMALE, SMCLE, SMRE/, SMWE/ (outputs)

All these pins are fully under firmware control, therefore timing compatibility is ensured by firmware only.

7.3. Serial slave synchronous interface

The SAM3703 can be controlled by an external host processor through this unidirectional serial interface. However, no firmware can be downloaded at power-up through this interface. Therefore an external ROM/Flash/EEPROM is required.

Pins used:
SCLK, SYNC, SDIN (input)
INT/ (output)

Data is shifted MSB first. The IC samples an incoming SDIN bit on the rising edge of SCLK, therefore the host should change SDIN on the negative SCLK edge.

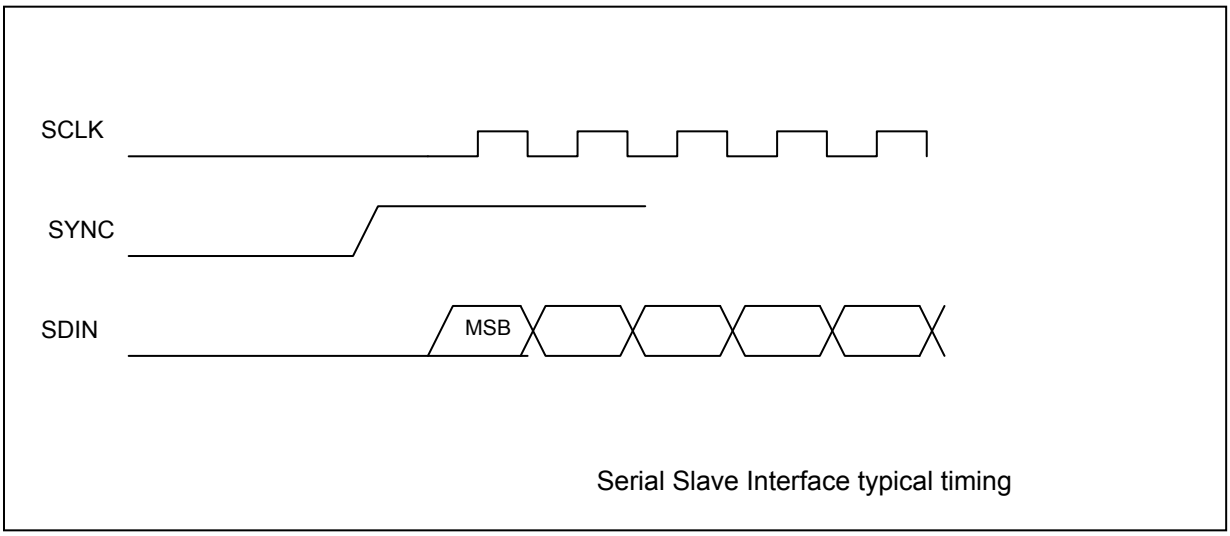
SYNC allows initial synchronization. The rising edge of SYNC, which should occur with SCLK low, indicates that SDIN will hold MSB data on the next rising SCLK.

The data is stored internally into a FIFO. Size of FIFO is firmware dependant. Minimum size is 128 bytes. Host should stop sending data as soon as INT/ goes high.

When the FIFO count is below 64, the INT/ output goes low. This allows the host processor to send data in burst mode.

The maximum SCLK frequency is fck (fck being the crystal frequency).
The minimum time between two bytes is 64 fck periods.

The contents of the SDIN data are defined by the firmware.



Serial Slave Interface typical timing

7.4. External DDR SDRAM and SDR SDRAM memories

7.4.1. Overview

The SAM3703 supports the DDR SDRAM components compatible with JEDEC standard (JESD79D).

Following memories can be connected to the SAM3703:

- DDR SDRAM, 4 bit wide
- SDRAM, 4 bit wide

DDR SDRAM and SDRAM cannot be connected at the same time. The type of connection is SSTL_2 for DDR SDRAM. and LVTTL for SDRAM.

DDR SDRAM and SDRAM use time multiplexed addressing with a ROW/COL scheme (banks WBA0 to WBA1 and address lines WA0 to WA11).

7.4.2. Double Data Rate SDRAM

Memory size

The data bus is 4 bits wide. Due to the 12-bit address bus, the maximum accessible address space is 128 Mbits (32M x 4). Larger components are supported, but only a part of address space will be used.

DDR Size	Bank address	Row address	Column address	Remark
64 Mbits (16M x 4)	2 bits	12 bits	10 bits	
128 Mbits (32M x 4)	2 bits	12 bits	11 bits	
256 Mbits (64M x 4)	2 bits	13 bits	11 bits	Only 12 bits row are used (only 128 Mbits are accessible).
512 Mbits (128 M x 4)	2 bits	13 bits	12 bits	
1 Gbits (256 M x4)	2 bits	14 bits	12 bits	Only 12 bits row are used (only 128 Mbits are accessible). Self-refresh might not be supported (according to tXSNR value; see below)

Pinning

SAM3703 pin	DDR pin	Description
-	A13, A12	Unused address bits (for larger device). Must be tied to zero.
WA11..WA0	A11..A0	Address
WBA1, WBA0	BA1, BA0	Bank address
WD3..WD0	DQ3..DQ0	Data
WDQS	DQS	Data strobe
	DM	Data mask. Must be tied to zero.
WCK, WCK/	CK, CK/	Differential clock
WCKE	CKE	Clock enable
-	CS/	Chip select. Must be tied to zero.
WCAS/	CAS/	Command
WRAS/	RAS/	
WWE/	WE/	
VREF	VREF	SSTL_2 reference voltage. Must be connected to 1.25 V.

Timing

General parameters

The DDR SDRAM is used with following parameters

Parameter		Symbol	Value
Clock cycle time		tCK	10 ns
Mode Register	CAS Latency	CL	2 cycles
	Burst length		4 data
	Burst type		sequential
	Operating mode		normal
Extended mode register	DLL		enabled
	Output drive strength		normal

Command sequencing

The SAM3703 supports DDR200 and faster DDR devices. This means that DDR device must support following parameters.

Parameter	Symbol	Value
MODE REGISTER SET command cycle time	tMRD	min 20 ns
ACTIVE to PRECHARGE command	tRAS	min 50 ns max 70 us
ACTIVE to ACTIVE/AUTO REFRESH command period	tRC	min 70 ns
AUTO REFRESH to ACTIVE/AUTO REFRESH command period	tRFC	min 120 ns
ACTIVE to READ or WRITE delay	tRCD	min 20 ns
PRECHARGE command period	tRP	min 20 ns
ACTIVE bank a to ACTIVE bank b command	tRRD	min 20 ns
WRITE recovery time	tWR	min 20 ns
Internal WRITE to READ command delay	tWTR	min 10 ns
Exit self refresh to non-READ command	tXSNR	min 80 ns
Exit self refresh to READ command	tXSRD	min 2 us
Average periodic REFRESH interval	tREFI	7.8 us

SAM3703 to DDR

Parameter	Symbol	Value
Address and control hold time	tIH	min 3.6 ns
Address and control setup time	tIS	min 3.2 ns
DQS falling edge to CK setup time	tDSS	min 4.3 ns
DQS falling edge hold time from CK	tDSH	min 4.3 ns
DQ and DM setup time	tDS	min 1.7 ns
DQ and DM hold time	tDH	min 0.8 ns

DDR to SAM3703

The data from DDR to SAM3703 must meet following timing requirements. These parameters are applicable at input of SAM3703, and must include effects of DDR device and effects of board layout.

Parameter	Symbol	Value
Skew between WDQS, WD3, WD2, WD1 and WD0	tDQSQ	max 1.6 ns
Delay from WCK, WCKN to WDQS (excluding CAS latency)	tDQSCK	max 5 ns

7.4.3. Single Data Rate SDRAM

Memory size

The data bus is 4 bits wide. Due to the 12-bit address bus, the maximum accessible address space is 128 Mbits (32M x 4). Larger components are supported, but only a part of address space will be used.

DDR Size	Bank address	Row address	Column address	Remark
64 Mbits (16M x 4)	2 bits	12 bits	10 bits	
128 Mbits (32M x 4)	2 bits	12 bits	11 bits	
256 Mbits (64M x 4)	2 bits	13 bits	11 bits	Only 12 bits row are used (only 128 Mbits are accessible).
512 Mbits (128 M x 4)	2 bits	13 bits	12 bits	

Pinning

SAM3703 pin	SDR pin	Description
-	A13, A12	Unused address bits (for larger device). Must be tied to zero.
WA11..WA0	A11..A0	Address
WBA1, WBA0	BA1, BA0	Bank address
WD3..WD0	DQ3..DQ0	Data
WDQS	-	Not used. Must be left unconnected.
	DM	Data mask. Must be tied to zero.
WCK	CK	Clock
WCK/	-	Not used. Must be left unconnected.
WCKE	CKE	Clock enable
-	CS/	Chip select. Must be tied to zero.
WCAS/	CAS/	Command
WRAS/	RAS/	
WWE/	WE/	
VREF	-	Must be connected to VC25/2.

Timing

General parameters

The SDR is used with following parameters

Parameter		Symbol	Value (50 MHz)	Value (100 MHz)
Clock cycle time		tCK	20 ns	10 ns
Mode Register	CAS Latency	CL	2 cycles	2 cycles
	Burst length		4 data	4 data
	Burst type		sequential	sequential
	Operating mode		normal	normal
	Output drive strength		normal	normal

Command sequencing

The SDR SDRAM device must support following parameters.

Parameter	Symbol	Value (50 MHz)	Value (100 MHz)
MODE REGISTER SET command cycle time	tMRD	min 40 ns	min 20 ns
ACTIVE to PRECHARGE command	tRAS	min 60 ns max 70 us	min 50 ns max 70 us
ACTIVE to ACTIVE/AUTO REFRESH command period	tRC	min 80 ns	min 70 ns
AUTO REFRESH to ACTIVE/AUTO REFRESH command period	tRFC	min 80 ns	min 70 ns
ACTIVE to READ or WRITE delay	tRCD	min 20 ns	min 20 ns
PRECHARGE command period	tRP	min 20 ns	min 20 ns
ACTIVE bank a to ACTIVE bank b command	tRRD	min 20 ns	min 20 ns
WRITE recovery time	tWR	min 20 ns	min 20 ns
Exit self refresh to non-READ command	tXSNR	min 80 ns	min 80 ns
Exit self refresh to READ command	tXSRD	min 4 us	min 2 us
Average periodic REFRESH interval	tREFI	7.8 us	7.8 us

SAM3703 to SDR SDRAM

The outputs of SAM3703 meet following constraints.

Parameter	Symbol	Value (50 MHz)	Value (100 MHz)
Address and control hold time	tIH	min 8.8 ns	min 3.8 ns
Address and control setup time	tIS	min 8.3 ns	min 3.3 ns
DQ and DM setup time	tDS	min 14.3 ns	min 6.8 ns
DQ and DM hold time	tDH	min 3.8 ns	min 1.4 ns

SDR to SAM3703

The data from SDR to SAM3703 must meet following timing requirements. These parameters are applicable at input of SAM3703, and must include effects of SDR device and effects of board layout.

Parameter	Symbol	Value
DQ setup time		min 2.0 ns
DQ hold time		min 1.8 ns

7.4.4. Address mapping

For information, following mapping is applied from internal Async bus address AAD[22:0] to SDRAM address.

SAM3703 Address Bus	Value at RAS time	Value at CAS time
WBA0	AAD0	AAD0
WBA1	AAD1	AAD1
WA0	AAD10	0 (see note)
WA1	AAD11	0 (see note)
WA2	AAD12	AAD2
WA3	AAD13	AAD3
WA4	AAD14	AAD4
WA5	AAD15	AAD5
WA6	AAD16	AAD6
WA7	AAD17	AAD7
WA8	AAD18	AAD8
WA9	AAD19	AAD9
WA10	AAD20	Auto-Precharge
WA11	AAD21	AAD22

Note: WA[1:0] = 00 at CAS time means that for each read or write operation at a specified address, four nibbles will be read or write in the burst sequential order (0,1,2,3). Other sequential orders are not allowed.

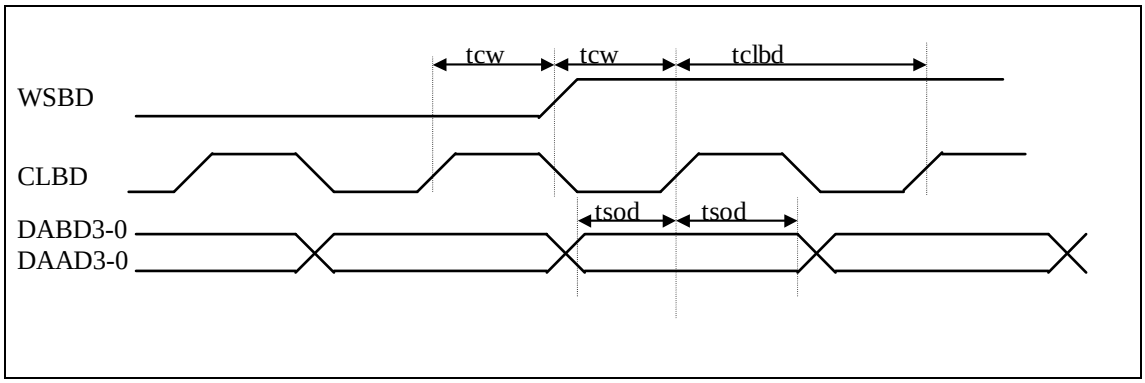
7.5. Digital audio

Pins used:
CLBD, WSBD (outputs)
DABD3-0 (outputs)
DAAD3-0 (inputs)

And optionally
CLAD3-0, WSAD3-0 (inputs)

The SAM3703 allows for 8 digital audio output channels and 8 digital audio input channels. All audio channels are normally synchronized on single clocks CLBD, WSBD which are derived from the IC crystal oscillator. However, as a firmware option, the DAAD3-0 inputs can be synchronized with incoming CLAD3-0 and WSAD3-0 signals. In this case, the incoming sampling frequencies must be lower or equal to the chip sampling frequency.

The digital audio timing follows the I2S standard, with up to 24 bits per sample



Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	tc-10	-	-	ns
DABD valid prior/after CLBD rising	tsod	tc-10	-	-	ns
CLBD cycle time	tclbd	-	2*tc	-	ns

tc is related to plck s follows:

Sample freq WSBD	Typ Sample Freq	tc	CLBD/WSBD freq ratio
1/(plck*512)	96kHz	4*plck	64
1/(plck*768)	64kHz	8*plck	48
1/(plck*1024	48kHz	8*plck	64
1/(plck*1536	32kHz	16*plck	48

Frame Format (FMT) is the number of plck cycles per digital audio frame. FMT is configurable by firmware. Possible values are: 512, 768, 1024, 1536

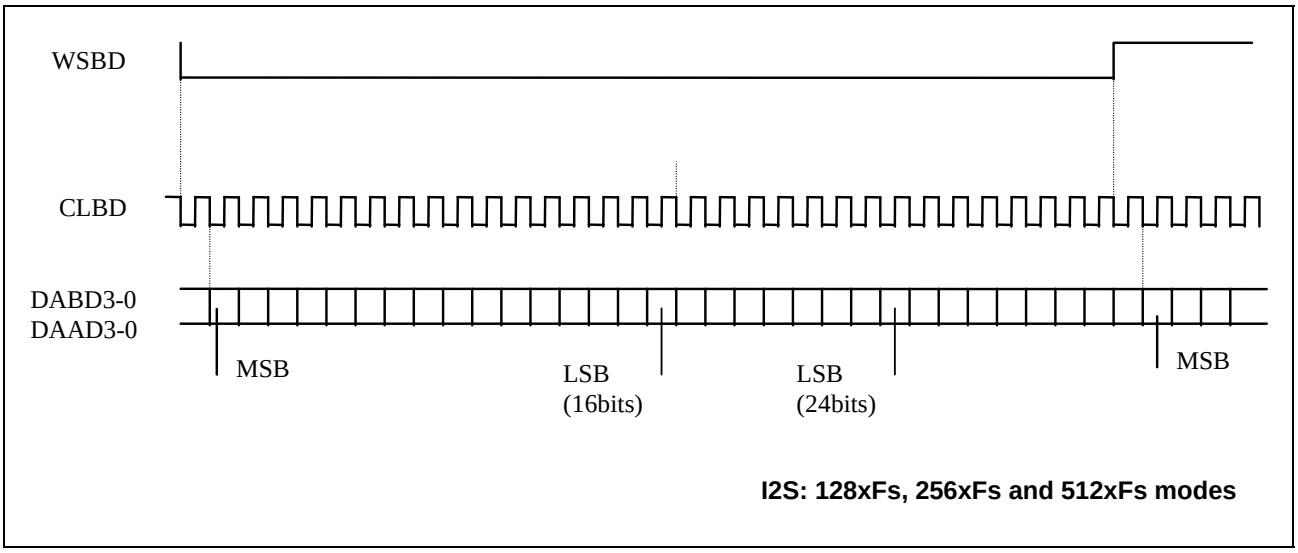
The choice of clock factors is done by the firmware. Speed option allows single or double speed mode for CKOUT. As an example, table below show all possible clock combinations with 12.288MHz Xtal.

plck value	CKOUT Speed	FMT	CKOUT/WSBD freq ratio	CLBD/WSBD freq ratio	fs @ Xtal=12.288MHz
tck/4	Single	1536	384	48	32kHz
tck/4	**Single**	**1024**	**256**	**64**	**48kHz (default)**
tck/4	Single	768	192	48	64kHz
tck/4	**Single**	**512**	**128**	**64**	**96kHz**
tck/4	Double	1536	768	48	32kHz
tck/4	**Double**	**1024**	**512**	**64**	**48kHz**
tck/4	Double	768	384	48	64kHz
tck/4	**Double**	**512**	**256**	**64**	**96kHz**

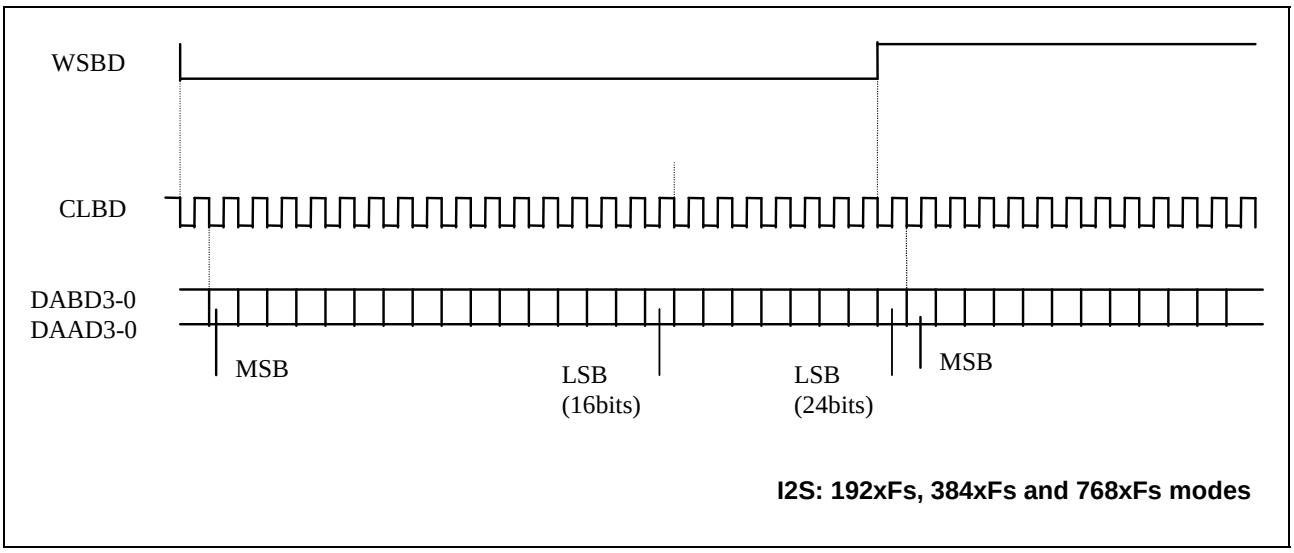
CKOUT speed (single or double) is defined by firmware

DIGITAL AUDIO FRAME FORMAT

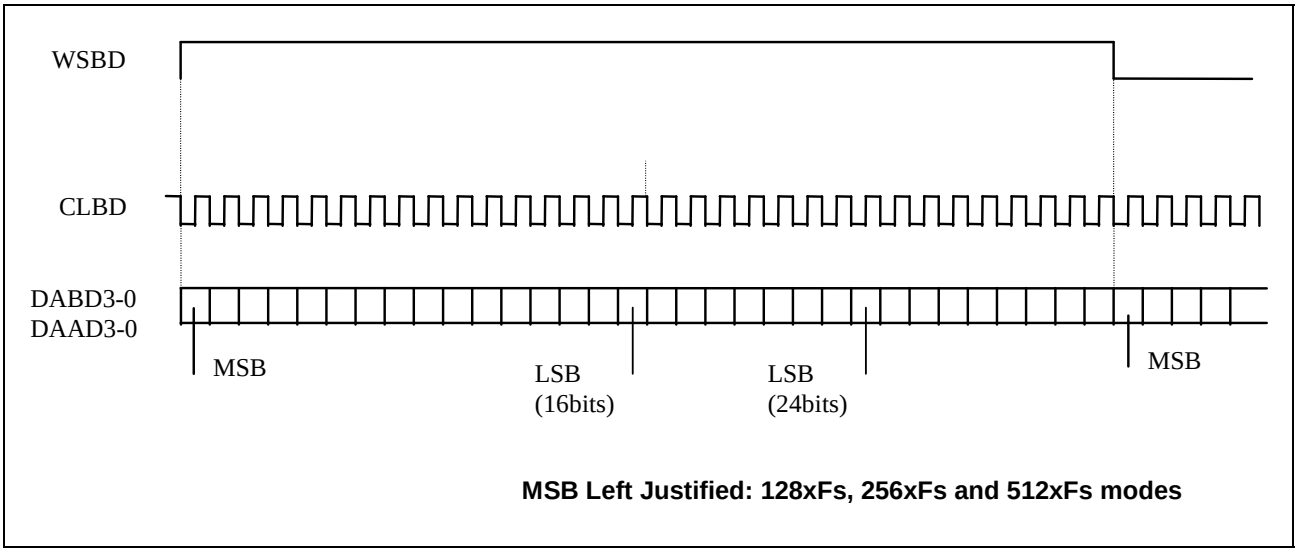
SAM3703 can generate I2S or MSB Left justified digital audio format. Master Clock can be 128xFs, 256xFs, 512xFs, 192xFs, 384xFS or 768xFs. Format and clock ratio are selected by firmware.



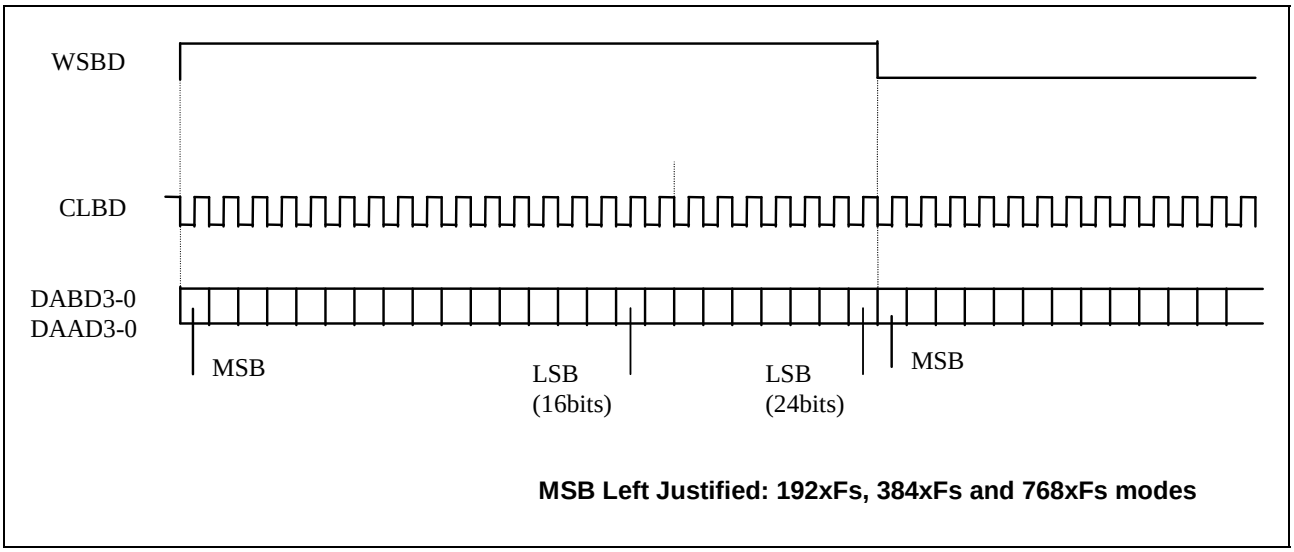
I2S: 128xFs, 256xFs and 512xFs modes



I2S: 192xFs, 384xFs and 768xFs modes



MSB Left Justified: 128xFs, 256xFs and 512xFs modes



MSB Left Justified: 192xFs, 384xFs and 768xFs modes

7.6. Serial MIDI_IN and MIDI_OUT

The serial MIDI IN and OUT signals are asynchronous signals following the MIDI transmission standard:

baud rate: programmable, typically 38.4kb/s
format: start bit(0), 8 data bits, stop bit(1)

8. Reset and Power Down

During power-up, the RESET/ input should be held low until the crystal oscillator and PLL are stabilized, which takes max. 10ms.
After the low to high transition of RESET/, following happens:

- All P24s enter an idle state.
- P16 program execution starts in built-in ROM.

The power-up sequence is as follows:

- STIN is sensed. If HIGH, then the built-in debugger is started.
- Addresses 0 &1 from internal EEPROM are checked. If “DR” is read, then control is transferred to address 400H from internal EEPROM.
- SMC/ is sensed. If LOW, then the built-in loader waits for SmartMedia presence detect (SMPD). When detected, the firmware is downloaded from SmartMedia reserved sector 1 and started.
- Firmware download from an host processor is assumed. (Download in 8k x 24 internal RAM)
  1. The byte 0ACh is written to the host, this rises IRQ. The host can recognize that the chip is ready to accept program download. Higher speed transfer can be reach by polling the parallel interface status (CS/=0, A0=1, RD/=0).
  2. The host sends the firmware size (in words) on two bytes (Low byte first).
  3. The host sends the SAM3703 firmware. The firmware should begin with string ”DR”.
  4. The byte 0ACh is written to the host, this rises IRQ. The host can recognize that the chip has accepted the firmware.
  5. SAM3703 starts the firmware.

If PDWN/ is asserted low, then the crystal oscillator and PLL are stopped. If the power switch is used, then the chip enters a deep power down sleep mode, as power is removed from the core. To exit power down, PDWN/ has to be asserted high, then RESET/ applied.

Other power reduction features allowing warm restart are controlled by firmware:

- P24s can be individually stopped
- The clock frequency can be internally divided by 256

9. Recommended Board Layout

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

- GND, VC33, VC25, VC18 distribution, decoupling

All GND, VC33, VC25, VC18 pins should be connected. A GND plane is strongly recommended. The board GND, VC33, VC25 and VC18 distribution should be in grid form.

Recommended VC18 decoupling is 0.1µF at each VC18 pin of the IC with an additional 10µFT decoupling close to the crystal. Minimum recommended VC25 decoupling is 0.1µF at pin 22, 42 and 55. VC33 requires a single 0.1µF decoupling.

- Crystal

The paths between the crystal, the crystal compensation capacitors and the IC should be short and shielded. The ground return from the compensation capacitors filter should be the GND plane from the IC.

- Busses

Parallel layout from D0-D7 and WA0-WA11/WDQ0-WDQ3 should be avoided. The D0-D7 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA0-WA11/WDQ0-WDQ3 which can corrupt address and/or data on these busses.

A ground plane should be implemented below the D0-D7 bus, which connects both to the host and to the IC GND.

A ground plane should be implemented below the WA0-WA11/WDQ0-WDQ3 bus, which connects both to the SDRAM or DDR SDRAM grounds and to the IC.

- DDR SDRAM and SDRAM

The routing of all signals must be as symmetric as possible. This applies particularly to WDQS, WDQ3, WDQ2, WDQ1 and WDQ0 signals.
The routing of all signals should be kept as short as possible.

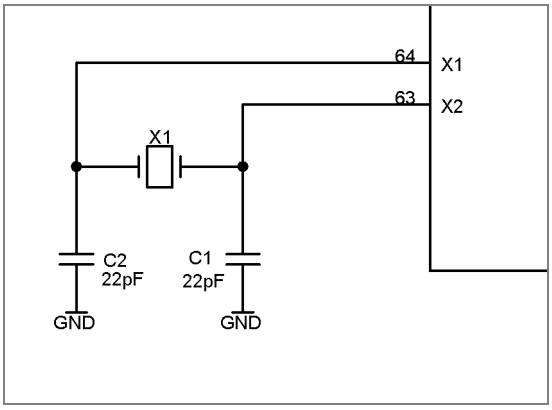
VREF must be equal to VC25/2, generated with a resistive divider. Both resistors must have the same value (1% precision). Suggested range is 50-150 Ω. Proper decoupling at each VREF pin (controller, VREF source and RAM device) is recommended.

The SSTL2 signals (DDR) must use a parallel termination (47 Ω, for example). This termination must be connected to VTT (VC25/2). This VTT is generated from a special component (able to source or to sink current) using VREF as reference. This termination must be placed just after DDR device.

- Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the Codec vendor recommended layout for correct implementation of the analog section.

10. Recommended Crystal Compensation



11. Product development and debugging

Dream provides an integrated product development and debugging tool SamVS. SamVS runs under Windows (98, ME, 2000, XP). Within the environment, it is possible to:

- Edit
- Assemble
- Debug on real target (In Circuit Emulation)
- Program internal EEPROM, SmartMedia on target.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using standard PC COM port communication at 57.6 kbauds. Thus time to market is optimized by testing directly on the final prototype.

A library of frequently used functions is available such as:

- Reverb
- Chorus
- Delay
- Compressor
- Pitch shifter
- Distortion
- Flanger
- Phaser
- Vocoder
- Feedback canceller
- MP3 decode
- 31 band equalizer
- Parametric equalizer

Dream engineers are available to study customer specific applications.

Dream Contact

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Website

http://www.dream.fr

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