SAM2653 Application Note

Migrate from SAM2553 to SAM2653

Overview

SAM2653 is the replacement for SAM2553. More than a simple shrunk version of SAM2553, SAM2653 also brings new features. This document describes the new features and helps migrating SAM2553 applications in SAM2653 applications.

Specifications comparison chart

FEATURES	SAM2553	SAM2653
Nominal Sampling Rate	48kHz	48kHz
Max Sound Bank	64MByte (512Mbit)	64MByte (512Mbit)
Max Keys	352	352
Max Switches	176	176
Max LEDs	88	88
Max ADC channels	16	16
LCD Display Interface	Yes	Yes
Package	LQFP128	LQFP128
Audio Out channels	4 (2 digital stereo)	4 (2 digital stereo)
Audio In channels	2 digital mono	2 digital mono
SPI	No	Yes
Debug/Program Interface	3-pin DBG-IF2 (quite slow)	2-pin DBG-IF3 (fast)
CDPG/ pin to avoid external logic ICs for debug	No	Yes
PRAM bit: Firmware can be run in internal RAM (e.g. for external Flash prog)	No	Yes
Reset and Power-down combined in one single pin	No	Yes

Package& Pinout

SAM2553 and SAM2653 are housed in the same LQFP128 package. However their pinout are different and not compatible.

Note: PCB should be redesigned when porting SAM2553 application to SAM2653.

SPI interface

A new SPI interface is now available on SAM2653 through dedicated pins SO, SI and SCK.
When SPI interface was needed with SAM2553, pins DB0, DB1 and RS were shared between LCD Display and SPI device. There are two possible way of migration on this point.

1) The DB0, DB1 and RS pins can be still use for SPI with SAM2653. The advantage is that no modification is needed in legacy firmware from SAM2553
2) Using the dedicated SPI controller on pins SO SI and SCLK pins needs to rework the SPI protocol in firmware but will freeing some P16 resources.

Note: No modification is needed on this point when porting SAM2553 firmware to SAM2653

Debug/Program interface

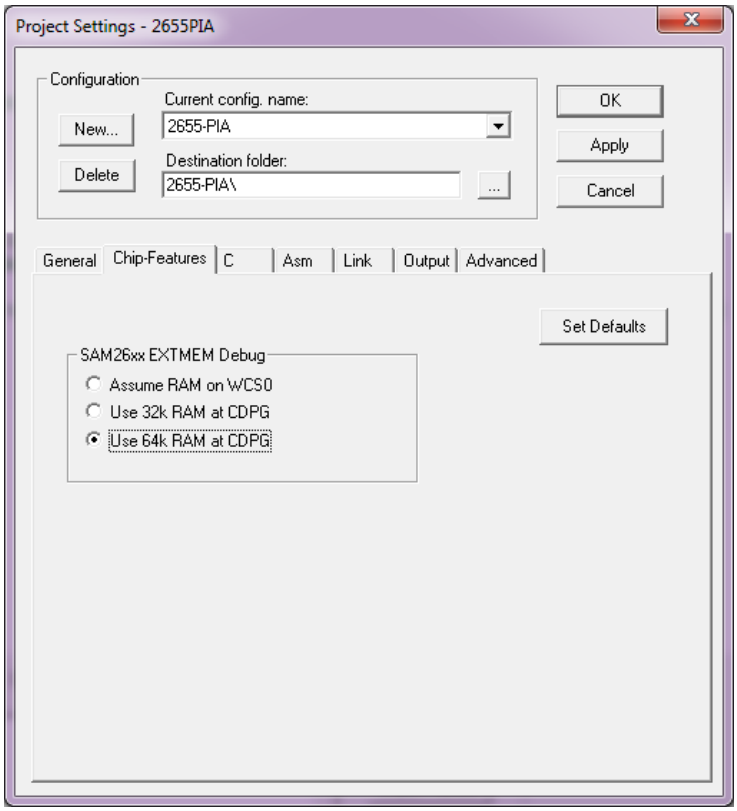
- SAM2553 debug interface is synchronous and based on pins DBDATA, DBACK, DBCLK.
  For debug, it is connected to DBG-IF2 port of USB-DBG-IF board.
- SAM2653 debug interface is asynchronous (57.6kbaud/s) and based on pins STIN, STOUT, FS0, FS1.
  For debug, it is connected to DBG-IF3 port of USB-DBG-IF board.

Note:

- *No modification is needed on this point when porting SAM2553 firmware to SAM2653*
- *Debug interface of SAM2653 is different from the one of SAM2553. Debug connector and connection of debug connector to SAM2653 are different. Pull-up/down resistors should be also added on FS0 (WA17) and FS1 (WA18) pins.*

Debug in external RAM - CDPG/ pin

- In SAM2553 application, external RAM for firmware debug is selected by an extra address decoding based on few logic ICs.
- In SAM2653 application, external RAM for firmware debug is selected by CDPG/ signal. CDPG/ is available as alternate function on pin XIO/. Settings for CDPG/ function are available in I/O PORT15 but they are automatically handled by SamVS. In SamVS, debug config can be set in Project Settings/Chip-Features tab.



The first option “Assume RAM on WCS0” allows having external address decoding for debug, like in SAM2553 applications.
It is recommended to use one of the CDPG options to avoid memory bus latencies due to extra external address decoding.

Note:

- *No modification is needed on this point when porting SAM2553 firmware to SAM2653*
- *Debug hardware can be simplified in SAM2653 environment by using new CDPG/ function.*

PRAM bit

Remapping first page (code page) to embedded RAM.
- If 0 first page mapped to external memory (WCS0).
- If 1 first page mapped to embedded 32kx16 RAM. Firmware can be run in internal RAM (e.g. for external Flash programming)

- SAM2653: PRAM bit is bit 4 In I/O PORT0
- SAM2553: PRAM bit is not implemented. Bit 4 In I/O PORT0 is always 0

Note: No modification is needed on this point when porting SAM2553 firmware to SAM2653

Reset and Power-down combined in one single pin

SAM2553: Reset is controlled by a dedicated pin RESET/. Power down mode is controlled by a dedicated pin PDWN/
SAM2653: Reset and Power-down mode are controlled by the same pin RST/PD/.

Note: No modification is needed on this point when porting SAM2553 firmware to SAM2653

Modified I/O Ports

PORT ADDRESS 0: CONFIGURATION WORD
Bit 4:
- SAM2553: Bit 4 is not used and should be always 0
- SAM2653: Bit4 is PRAM
  PRAM:
  Remapping first page to embedded RAM.
  - If 0 first page mapped to external memory (WCS0).
  - If 1 first page mapped to embedded 32kx16 RAM

PORT ADDRESS 15: SYSTEM CONTROL/STATUS
Bit [3:0]:
- SAM2553: asynchronous debug interface (DBOUTEN, DBACK, DBOUT, DBCLK, DBIN)
- SAM2653: synchronous debug interface status (TINPIN, TOUTRQST, TINRDY)
  TINRDY: Set when a byte is received on the STIN pin.
  TOUTRQST: Set when a byte can be transmitted to STOUT.
  TINPIN: Value of STIN pin.

Bit 6:
- SAM2553:unused bit
- SAM2653:
  XIOALT: Alternate function setting for XIO/ pin
  - 0 for XIO/ function
  - 1 for CDPG/ function

Bit 7:
- SAM2553:unused bit
- SAM2653:
  CDSZ: Define max code size for debug with external RAM.
  - 0 for code size max = 0x10000
  - 1 for code size max = 0x08000

Bit 8:
- SAM2553:unused bit
- SAM2653:
  TESTEN: Enable test timer and test serial port STIN/STOUT

Bit 9:
- SAM2553:unused bit
- SAM2653:

  FS READ: Freq Sense Read
  - 1 for Freq Sense reading. WA[18:17] pins configured as input.
    Current Freq Sense FS[1:0]=WA[18:17] can be read on bits 11 and 10
  - Toggle from 1 to 0 for Freq Sense capture.
    FS[1:0] values are captured and stored on bits 11 and 10
  - 0 for normal mode: WA[18:17] pins configured as output.

Bit [11:10]:
- SAM2553:unused bit
- SAM2653:

  FS[1:0]: Frequency Sense
  - if FSREAD=1: Current Freq Sense value on WA[18:17] pins
  - if FSREAD=0: Freq Sense value captured on WA[18:17] pins at latest FSREAD state change from 1 to 0.

Bit 13:
- SAM2553:unused bit
- SAM2653:

  RAMDBG: Set if external RAM used for debug. Size of external RAM defined in bit CDSZ. CS/ pin of debug RAM should be connected to SAM26xx CDPG/ pin.

Note: No modification is needed on this point when porting SAM2553 firmware to SAM2653

New I/O Ports

PORT ADDRESS 28: SPI CONTROL
PORT ADDRESS 29: SPI DATA
PORT ADDRESS 250: HARDWARE SIGNATURE
PORT ADDRESS 254: TEST UART – BAUD RATE GENERATOR
PORT ADDRESS 250: TEST UART – DATA IN/OUT

Note:
- *See ProgRef26xx.pdf for new I/O ports description.*