SAM5704B Application Note

Migrate from SAM5704 to SAM5704B

Overview

SAM5704B is a shrunk, low-power, version of SAM5704. Backward compatibility of standard designs based on SAM5704 is normally ensured. However, before migration, it is safe to check that the minor differences between SAM5704 and SAM5704B will be supported in each design.

Differences between SAM5704 and SAM5704B

1. Consumptions

Consumptions in SAM5704B are lowers than in SAM5704. See table below.

Parameter	Symbol	SAM5704			SAM5704B			Unit
		Min	Typ	Max	Min	Typ	Max	
VD33 power supply current in warm power down (PLL stopped, Sys clk = 12.288MHz crystal, all P24 stopped)	ID33	-	8.9	-	-	6	-	mA
VD33 power supply current in reset mode (RST/=0)	ID33	-	3.6	-	-	0.6	-	mA
VD33 power supply current (crystal freq.= 12.288 MHz, all P24 stopped, SDR=Off)	ID33		101			34		mA
VD33 power supply current (crystal freq.= 12.288 MHz, all P24 stopped, SDR=On)	ID33		112			54		mA
VD33 power supply current (crystal freq.= 12.288 MHz, all P24 running, SDR=On)	ID33		140			96		mA
VM power supply current (crystal freq.= 12.288 MHz, VM=3.3V, SDR SDRAM)	IDM	21	-	44	21	-	44	mA
VM power supply current in reset mode	IDM	-	-	<1	-	-	<1	µA
VA33 power supply current (ADC running @ 11MHz)	IA33	-	3.2	-	-	3.2	-	mA
VA33 power supply current in reset mode	IA33	-	-	<1	-	-	<1	µA
USB Full Speed current	ID33U	-	18	-	-	16	-	mA
USB High Speed current	ID33U	-	29	-	-	29	-	mA
Ethernet MAC current	ID33E	-	15	-	-	15	-	mA

2. VM power supply removal

In SAM5704 there are VM power supply pins. VM power supply is dedicated to parallel memory interface (NOR Flash, SRAM, SDRAM)
In case of SAM5704B, VM pins have been replaced by VD33 pins.

Pin#	Power supply Name and Range		Note
	SAM5704	SAM5704B	
12, 19, 27, 34, 41, 48, 62	VM 3V<VM<3.6V	VD33 3V<VD33<3.6V	Full compatibility

3. Pads properties

IO pads of some pins have different properties in SAM5704 and SAM5704B. Table below lists all of them.

5VT indicates a 5 volt tolerant Input or I/O pin.
DR4, DR8, DR12 indicates driving capability at VOL, VOH (e.g., DR8 means IOH and IOL = 8mA Max)
MEM indicates a memory pad supplied by VM in SAM5704 (IOH and IOL = 20mA Max, Non 5-volt tolerant)

Pin#	Pad Properties		Primary Function					
	SAM5704	SAM5704 B	Mem Cfg1	Mem Cfg2	Mem Cfg3	Mem Cfg4	Mem Cfg5	Mem Cfg6
4	I/O DR4	I/O 5VT DR4	STOUT	STOUT	STOUT	STOUT	STOUT	STOUT
7	I/O DR8	I/O 5VT DR8	SPICK	SPICK	SPICK	SPICK	SPICK	SPICK
8	I/O DR8	I/O 5VT DR8	SPICS0/	SPICS0/	SPICS0/	SPICS0/	SPICS0/	SPICS0/
10	I/O DR4	I/O 5VT DR12	NRCS0/	NRCS0/	DAAD0	DAAD0	DAAD0	QSRCS/
11	I/O DR12	I/O 5VT DR12	NRCS1/	NRCS1/	DABD0	DABD0	DABD0	QNRCS0/
13	I/O MEM DR20	I/O 5VT DR12	DRCAS/	CS/	DRCAS/	CS/	CS/	CS/
14	I/O MEM DR20	I/O 5VT DR12	DRRAS/	RD/	DRRAS/	RD/	RD/	RD/
15	I/O MEM DR20	I/O 5VT DR12	DRWE/	WR/	DRWE/	WR/	WR/	WR/
16	I/O MEM DR20	I/O 5VT DR12	DRCKE	IRQ	DRCKE	IRQ	IRQ	IRQ
17	I/O MEM DR20	I/O 5VT DR12	DRCS0/	DABD3	DRCS0/	DABD3	MDC	MDC
18	I/O MEM DR20	I/O 5VT DR12	DRCS1/	DAAD1	DRCS1/	DAAD1	MDIO	MDIO

(To be continued)

(Continued)

Pin#	Pad Properties		Primary Function					
	SAM5704	SAM5704B	Mem Cfg1	Mem Cfg2	Mem Cfg3	Mem Cfg4	Mem Cfg5	Mem Cfg6
20	I/O MEM DR20	I/O 5VT DR12	MA0	MA0	MA0	MA0	MA0	D0
21	I/O MEM DR20	I/O 5VT DR12	MA1	MA1	MA1	MA1	MA1	D1
22	I/O MEM DR20	I/O 5VT DR12	MA2	MA2	MA2	MA2	MA2	D2
23	I/O MEM DR20	I/O 5VT DR12	MA3	MA3	MA3	MA3	MA3	D3
25	I/O MEM DR20	I/O 5VT DR12	DRDM0	A0	DRDM0	A0	A0	A0
26	I/O MEM DR20	I/O 5VT DR12	DRDM1	DABD1	DRDM1	DABD1	DABD1	DAAD1
28	I/O MEM DR20	I/O 5VT DR12	DRCK	DABD2	DRCK	DABD2	DABD2	DABD2
29	I/O MEM DR20	I/O 5VT DR12	MD0	MD0	MD0	MD0	MD0	QNR0
30	I/O MEM DR20	I/O 5VT DR12	MD1	MD1	MD1	MD1	MD1	QNR1
31	I/O MEM DR20	I/O 5VT DR12	MD2	MD2	MD2	MD2	MD2	QNR2
32	I/O MEM DR20	I/O 5VT DR12	MD3	MD3	MD3	MD3	MD3	QNR3
35	I/O MEM DR20	I/O 5VT DR12	MD4	MD4	MD4	MD4	MD4	QNR4
36	I/O MEM DR20	I/O 5VT DR12	MD5	MD5	MD5	MD5	MD5	QNR5
37	I/O MEM DR20	I/O 5VT DR12	MD6	MD6	MD6	MD6	MD6	QNR6
38	I/O MEM DR20	I/O 5VT DR12	MD7	MD7	MD7	MD7	MD7	QNR7
39	I/O MEM DR20	I/O 5VT DR12	MD8	MD8	MD8	MD8	MD8	QSR0
40	I/O MEM DR20	I/O 5VT DR12	MD9	MD9	MD9	MD9	MD9	QSR1
42	I/O MEM DR20	I/O 5VT DR12	MD10	MD10	MD10	MD10	MD10	QSR2
43	I/O MEM DR20	I/O 5VT DR12	MD11	MD11	MD11	MD11	MD11	QSR3
44	I/O MEM DR20	I/O 5VT DR12	MD12	MD12	MD12	MD12	MD12	SPI0
45	I/O MEM DR20	I/O 5VT DR12	MD13	MD13	MD13	MD13	MD13	SPI1
46	I/O MEM DR20	I/O 5VT DR12	MD14	MD14	MD14	MD14	MD14	SPI2
47	I/O MEM DR20	I/O 5VT DR12	MD15	MD15	MD15	MD15	MD15	SPI3
49	I/O MEM DR20	I/O 5VT DR12	MA4	MA4	MA4	MA4	MA4	D4
50	I/O MEM DR20	I/O 5VT DR12	MA5	MA5	MA5	MA5	MA5	D5
51	I/O MEM DR20	I/O 5VT DR12	MA6	MA6	MA6	MA6	MA6	D6
52	I/O MEM DR20	I/O 5VT DR12	MA7	MA7	MA7	MA7	MA7	D7
53	I/O MEM DR20	I/O 5VT DR12	MA8	MA8	MA8	MA8	MA8	TXD0
54	I/O MEM DR20	I/O 5VT DR12	MA9	MA9	MA9	MA9	MA9	TXD1
56	I/O MEM DR20	I/O 5VT DR12	MA10	MA10	MA10	MA10	MA10	RXD0
57	I/O MEM DR20	I/O 5VT DR12	MA11	MA11	MA11	MA11	MA11	RXD1
58	I/O MEM DR20	I/O 5VT DR12	MA12	MA12	MA12	MA12	MA12	TX_EN
59	I/O MEM DR20	I/O 5VT DR12	MA13	MA13	MA13	MA13	MA13	CRS_DV
60	I/O MEM DR20	I/O 5VT DR12	MA14	MA14	MA14	MA14	MA14	RX_ER
61	I/O MEM DR20	I/O 5VT DR12	MA15	MA15	MA15	MA15	MA15	ETH_RES/
69	I/O DR4 DR20	I/O 5VT DR8	DABD1	SRCS/	DABD1	SRCS/	SRCS/	DABD1
70	I/O DR12	I/O 5VT DR8	DAAD2	DAAD2	DAAD2	DAAD2	REF_CLK	REF_CLK
74	I/O DR12	I/O 5VT DR8	MWE/	MWE/	IRQ	MWE/	MWE/	QSRCK
98	I/O DR12	I/O 5VT DR12	DABD0	DABD0	NDCE0/	NDCE0/	DABD3	DABD0
99	I/O DR4	I/O 5VT DR12	DAAD0	DAAD0	NDCE1/	NDCE1/	DAAD2	DAAD0
104	I/O DR4	I/O 5VT DR8	A0	DABD6	NDRE/	NDRE/	DAAD3	QNRCK
107	I/O 5VT DR8	I/O 5VT DR12	SPI1	SPI1	SPI1	SPI1	SPI1	BR1
108	I/O 5VT DR8	I/O 5VT DR12	SPI2	SPI2	SPI2	SPI2	SPI2	BR2
109	I/O 5VT DR8	I/O 5VT DR12	SPI3	SPI3	SPI3	SPI3	SPI3	BR3
118	I/O DR4	I/O 5VT DR8	D7	D7	NDIO7	NDIO7	D7	QNRCS1/

Pads properties on SAM5704B should be compatible with the ones of SAM5704 in most of cases. However this compatibility is schematic dependent and should be rechecked for each application.

4. Safe ROM boot

At start-up boot loader tries to locate firmware from various interfaces. To avoid conflicts, serial resistor should be added on some pins if they are used as GPIO input.
In SAM5704B, one potential conflict has been removed on MA16-MA26 pins when they are used as GPIO.
Consequence is:
- SAM5704: If MA16-MA26 pins are used as GPIO input, an external 330Ω (min) serial resistor is needed for safe ROM boot.
- SAM5704B: If MA16-MA26 pins are used as GPIO input, no external serial resistor is needed.

Safe ROM boot rules for SAM5704B are compatible with the ones for SAM5704.

5. SPDIF swap

- In SAM5704, SPDIF Input or Output are available on some pins as secondary function
- In SAM5704B, SPDIF Input or Output are available on same pins as secondary function but there is a new SWAP_SPDIF feature activated by setting bit 13 in IO register.

Primary function Name	Secondary function Name		SWAP_SPDIF Value	SPDIF Direction
	SAM5704	SAM5704B		
SPI0	SPDIF_OUT	SPDIF_OI	0	Output
			1	Input
SPI1	SPDIF_IN	SPDIF_IO	0	Input
			1	Output
SPI3	SPDIF_IN	SPDIF_IO	0	Input
			1	Output
DAAD0	SPDIF_IN	SPDIF_IO	0	Input
			1	Output
DABD0	SPDIF_OUT	SPDIF_OI	0	Output
			1	Input

SPDIF implementation in SAM5704B is compatible with the one of SAM5704.

6. Firmware download from Host

- At start-up SAM5704 can download its firmware from a host connected to 8-bit parallel interface
- At start-up SAM5704B can download its firmware from a host connected to 8-bit parallel interface or connected to Serial Slave Synchronous interface or to MIDI_IN1. By default, 8-bit parallel interface and MIDI_IN1 are together activated. Serial Slave Synchronous interface can be activated instead of 8-bit parallel by blowing the “SSS” eFuse.

SAM5704 and SAM5704B are compatible for firmware download from a host connected to 8-bit parallel interface